FIG. 1

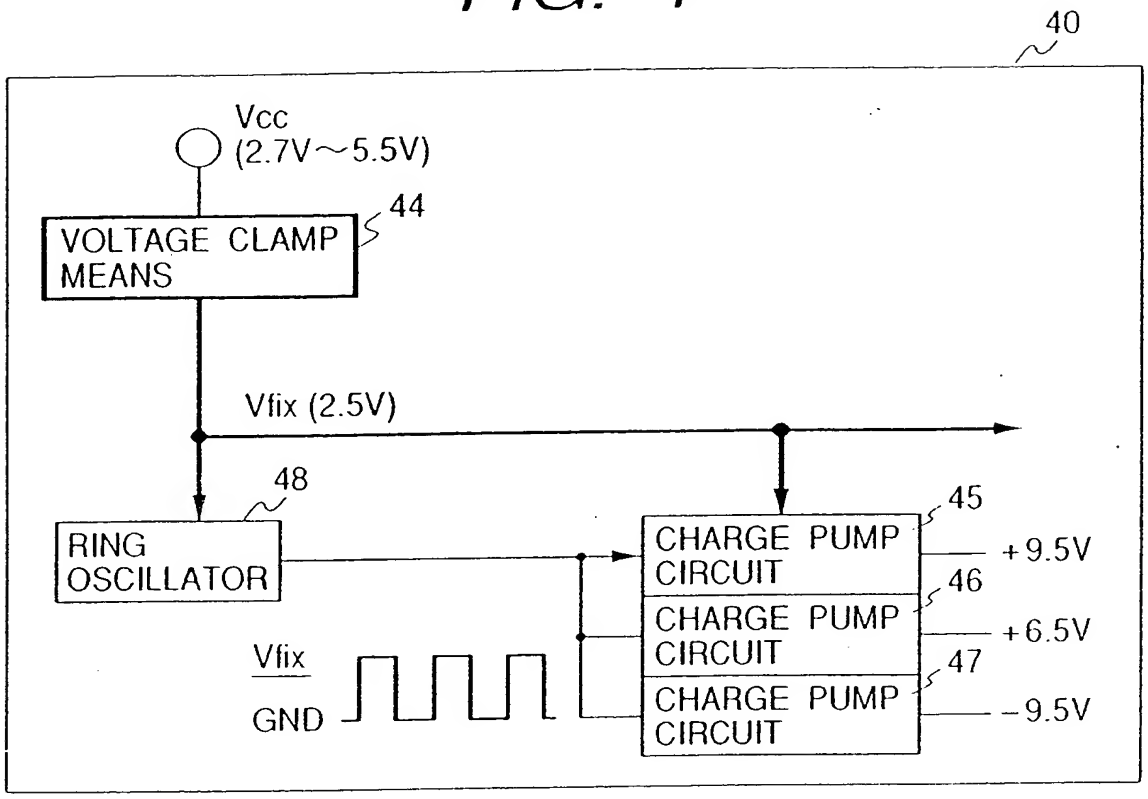



FIG. 2
PRIOR ART

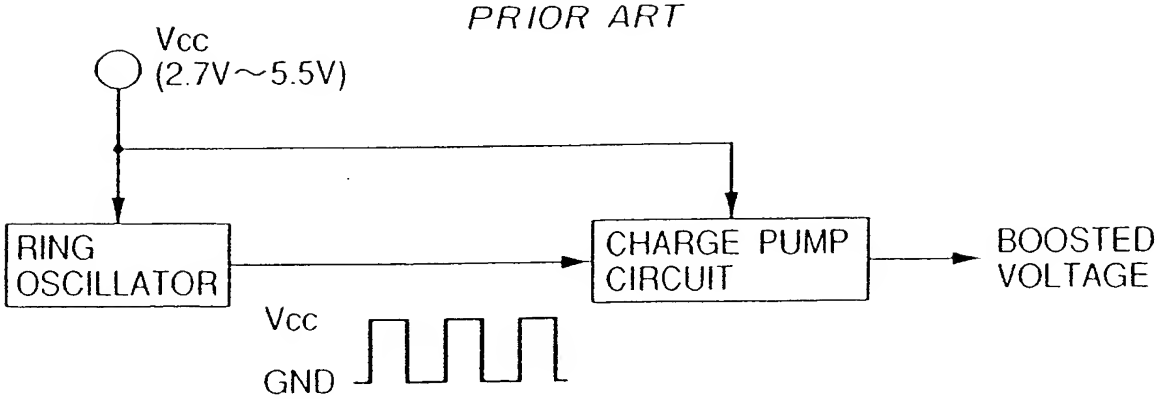


FIG. 3

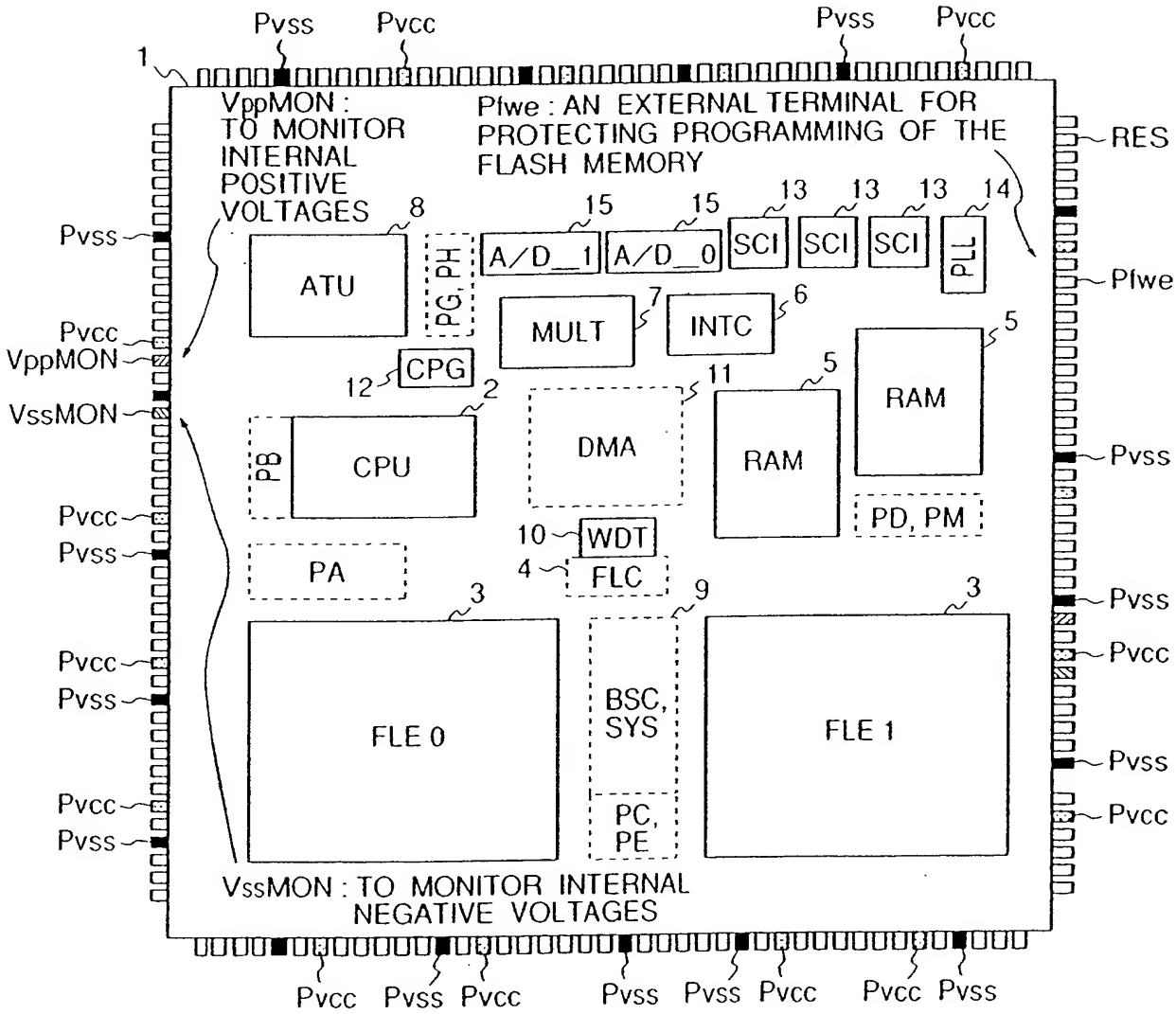
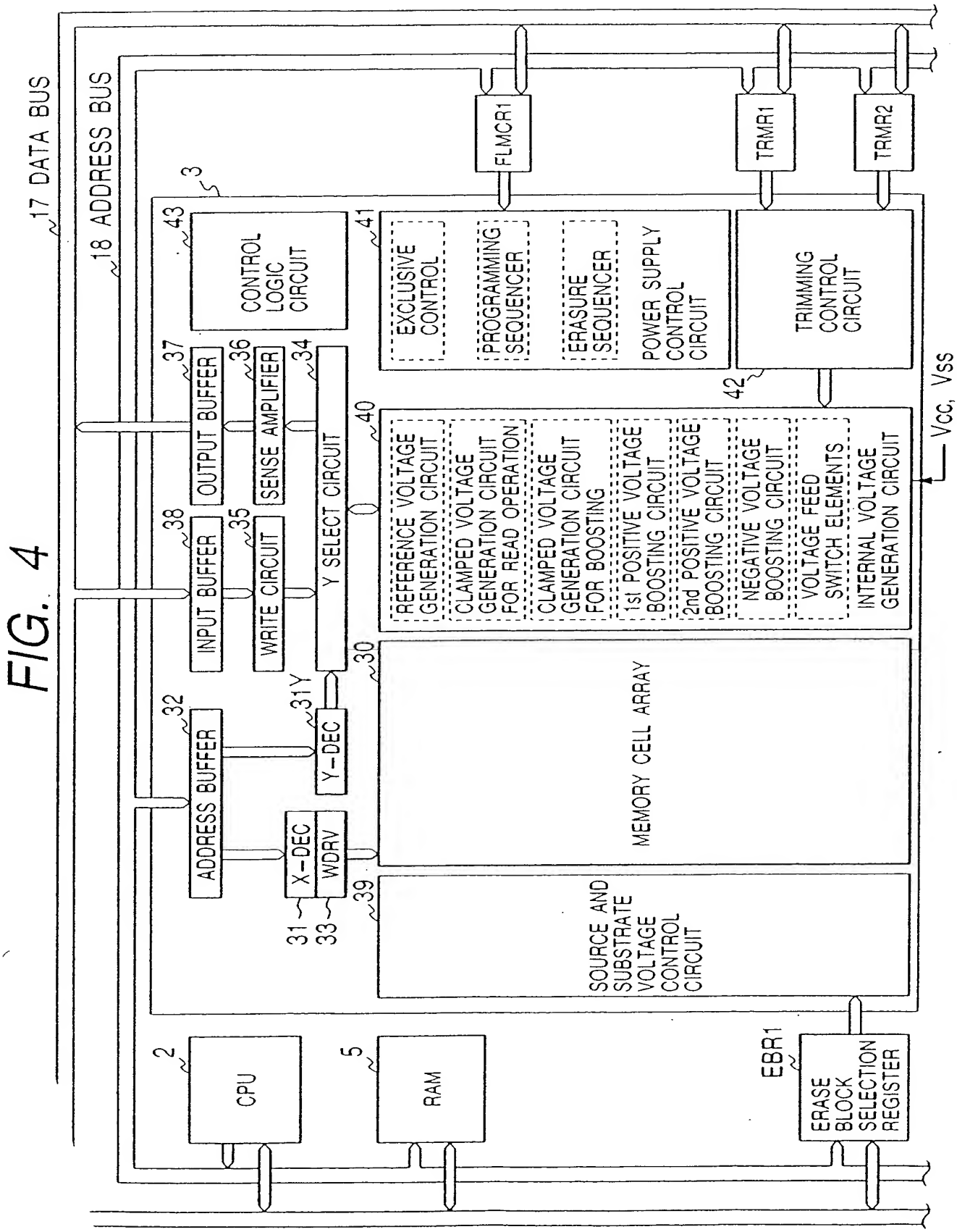

Pvss
Pvcc
Pvss
Pvcc
1
VppMON : TO MONITOR INTERNAL POSITIVE VOLTAGES
Pfwe : AN EXTERNAL TERMINAL FOR PROTECTING PROGRAMMING OF THE FLASH MEMORY
RES
Pfwe
Pvss
Pvcc
VppMON
VssMON
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
Pvcc
Pvss
8
ATU
PG, PH
15
A/D_1
15
A/D_0
13
SCI
13
SCI
13
SCI
14
PLL
7
MULT
6
INTC
5
RAM
12
CPG
2
CPU
PB
11
DMA
5
RAM
PD, PM
10
WDT
4
FLC
PA
3
FLE 0
9
BSC, SYS
PC, PE
3
FLE 1
VssMON : TO MONITOR INTERNAL NEGATIVE VOLTAGES
Pvcc
Pvss
Pvcc
Pvss
Pvss
Pvcc
Pvcc
Pvss

FIG. 4


17 DATA BUS
18 ADDRESS BUS
3
43
CONTROL LOGIC CIRCUIT
41
EXCLUSIVE CONTROL
PROGRAMMING SEQUENCER
ERASURE SEQUENCER
POWER SUPPLY CONTROL CIRCUIT
FLMCR1
TRMR1
TRMR2
TRIMMING CONTROL CIRCUIT
42
37
OUTPUT BUFFER
36
SENSE AMPLIFIER
34
Y SELECT CIRCUIT
40
REFERENCE VOLTAGE GENERATION CIRCUIT
CLAMPED VOLTAGE GENERATION CIRCUIT FOR READ OPERATION
CLAMPED VOLTAGE GENERATION CIRCUIT FOR BOOSTING
1st POSITIVE VOLTAGE BOOSTING CIRCUIT
2nd POSITIVE VOLTAGE BOOSTING CIRCUIT
NEGATIVE VOLTAGE BOOSTING CIRCUIT
VOLTAGE FEED SWITCH ELEMENTS
INTERNAL VOLTAGE GENERATION CIRCUIT
Vcc, Vss
38
INPUT BUFFER
35
WRITE CIRCUIT
31Y
Y-DEC
30
MEMORY CELL ARRAY
32
ADDRESS BUFFER
X-DEC
WDRV
31
33
39
SOURCE AND SUBSTRATE VOLTAGE CONTROL CIRCUIT
2
CPU
5
RAM
EBR1
ERASE BLOCK SELECTION REGISTER

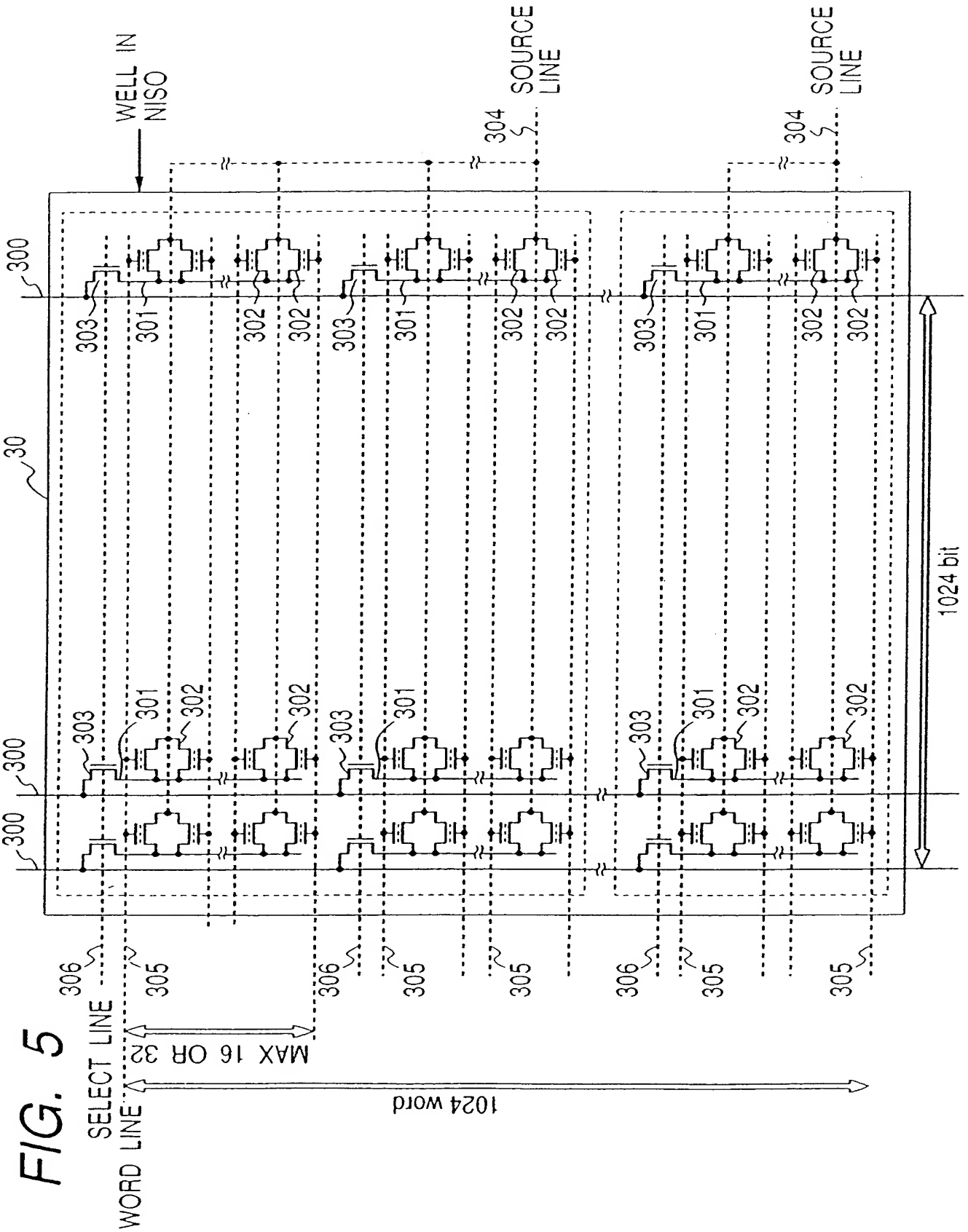

WELL IN
NISO
SOURCE LINE
SOURCE LINE
304
304
300
300
300
30
303
301
302
302
303
301
302
302
303
301
302
302
303
301
302
302
303
301
302
302
303
301
302
302
1024 bit
306
305
306
305
305
306
305
305
SELECT LINE
WORD LINE
MAX 16 OR 32
1024 word

FIG. 5

FIG. 6

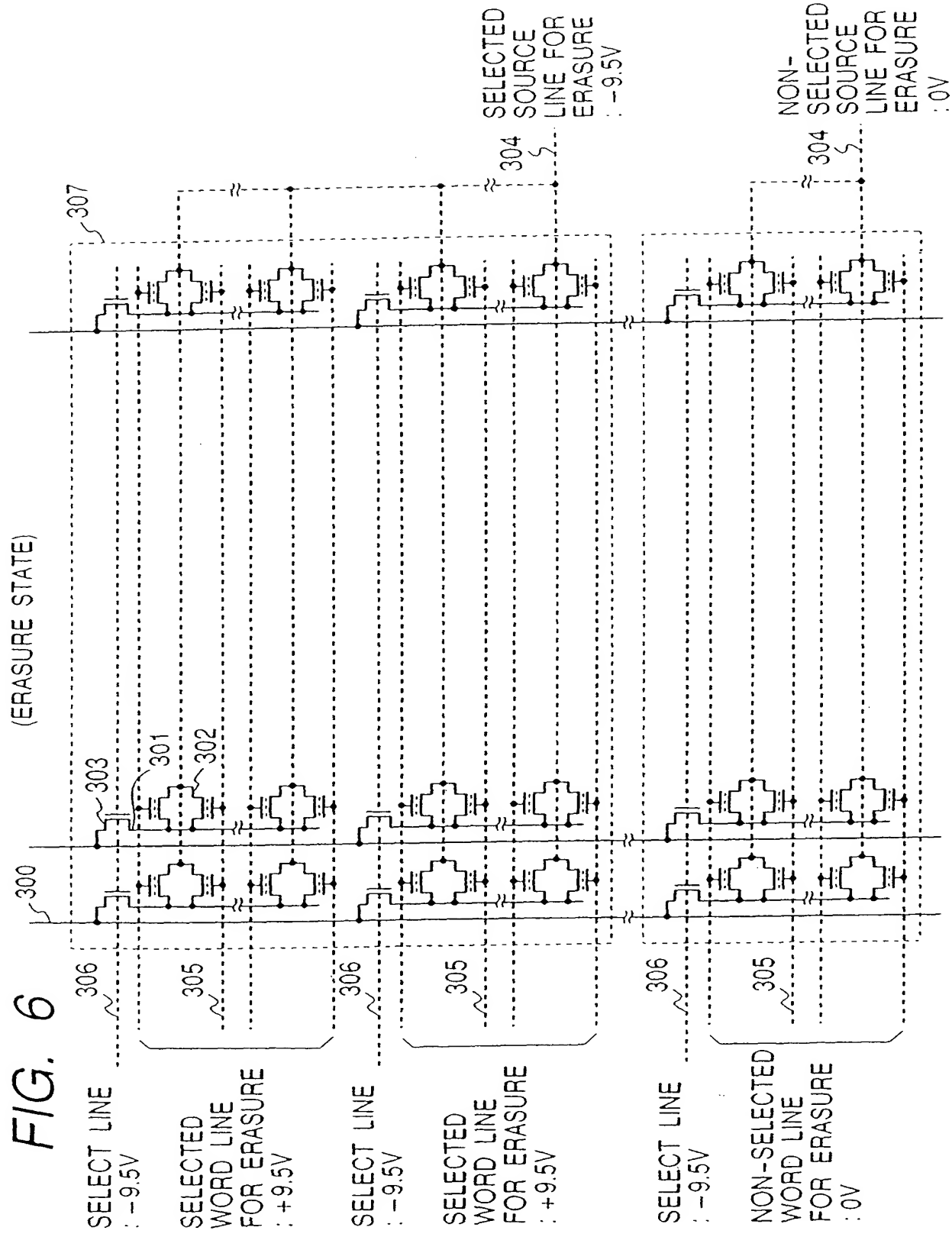

(ERASURE STATE)
SELECT LINE : -9.5V
SELECTED WORD LINE FOR ERASURE : +9.5V
SELECT LINE : -9.5V
SELECTED WORD LINE FOR ERASURE : +9.5V
SELECT LINE : -9.5V
NON-SELECTED WORD LINE FOR ERASURE : 0V
SELECTED SOURCE LINE FOR ERASURE : -9.5V
NON-SELECTED SOURCE LINE FOR ERASURE : 0V
300
301
302
303
304
305
306
307

FIG. 7

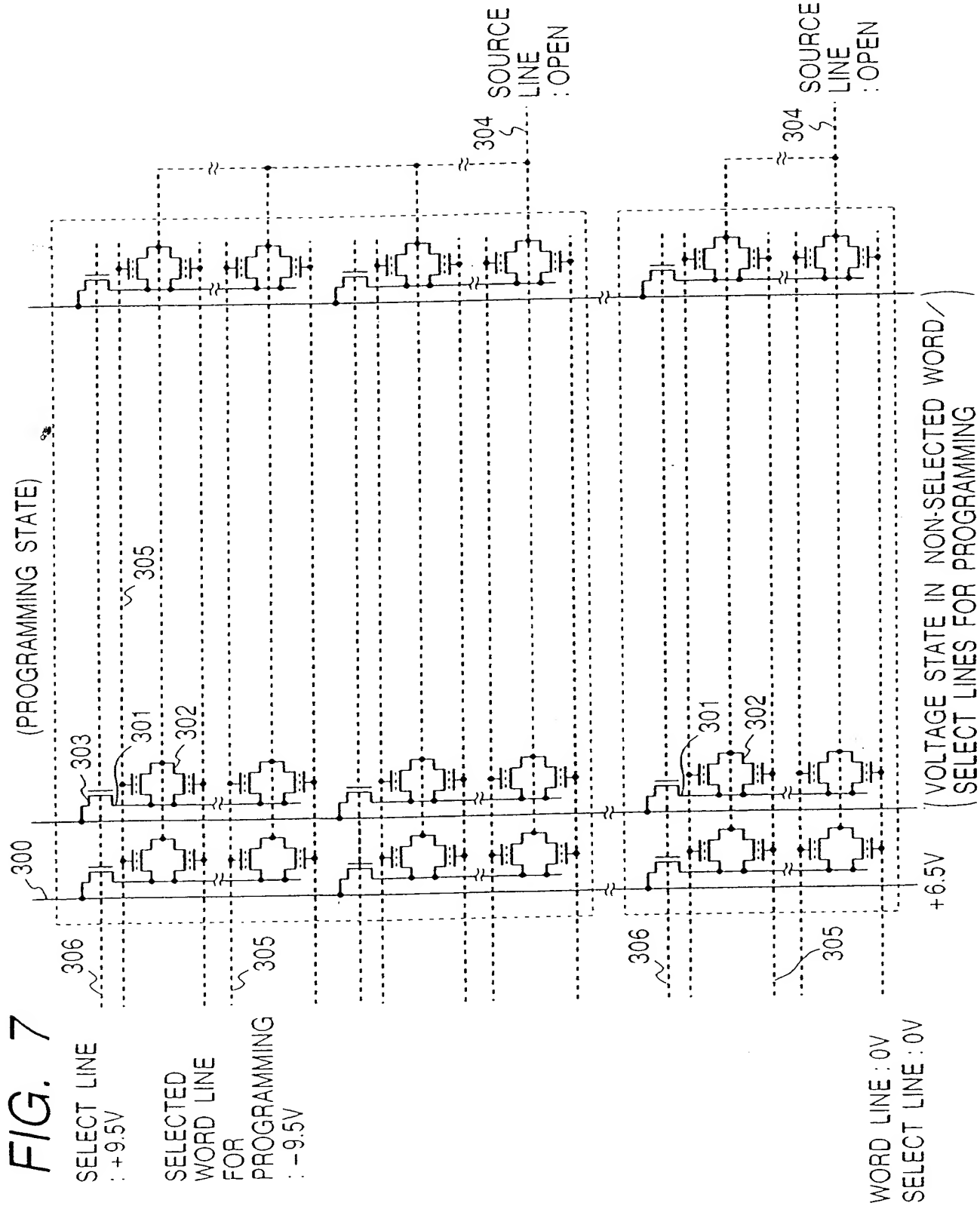

(PROGRAMMING STATE)
SELECT LINE : +9.5V
SELECTED WORD LINE FOR PROGRAMMING : -9.5V
WORD LINE : 0V
SELECT LINE : 0V
SOURCE LINE : OPEN
SOURCE LINE : OPEN
VOLTAGE STATE IN NON-SELECTED WORD/SELECT LINES FOR PROGRAMMING
+6.5V
300
301
302
303
304
305
306

FIG. 8

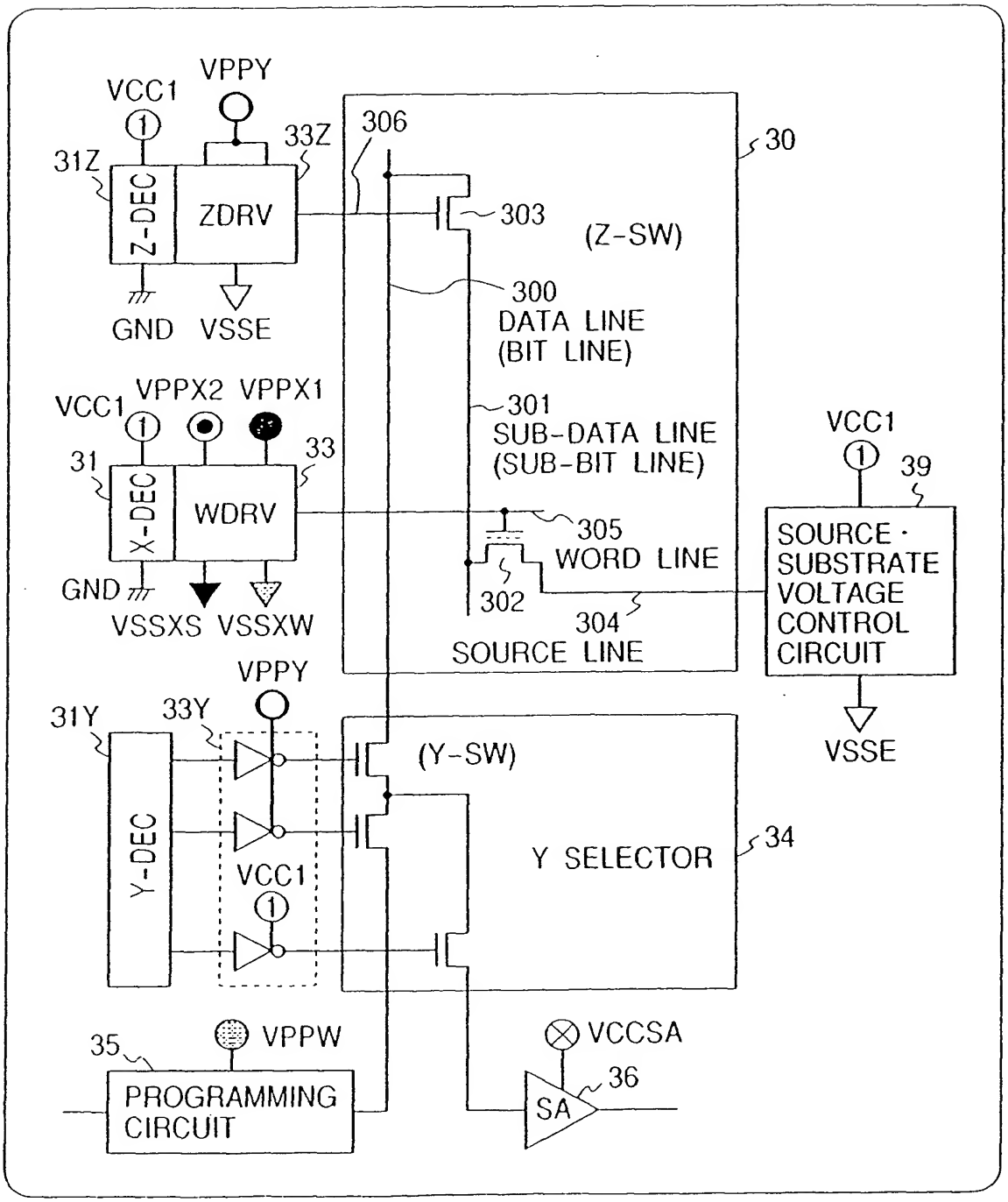

VCC1
VPPY
31Z
33Z
306
30
Z-DEC
ZDRV
303
(Z-SW)
GND
VSSE
300
DATA LINE
(BIT LINE)
VCC1
VPPX2
VPPX1
301
SUB-DATA LINE
(SUB-BIT LINE)
31
33
X-DEC
WDRV
305
WORD LINE
GND
VSSXS
VSSXW
302
304
SOURCE LINE
VCC1
39
SOURCE · SUBSTRATE VOLTAGE CONTROL CIRCUIT
VSSE
VPPY
31Y
33Y
(Y-SW)
Y-DEC
VCC1
Y SELECTOR
34
35
VPPW
PROGRAMMING CIRCUIT
VCCSA
36
SA

FIG. 9

| SYMBOL | NAME | REMARK |
|---|---|---|
| ○ | VCC | Vcc SUPPLY |
| ⏚ | GND | GND SUPPLY |
| ● | VPPX1 | POSITIVE VOLTAGE SUPPLY 1 ON WORD DRIVERS |
| ◉ | VPPX2 | POSITIVE VOLTAGE SUPPLY 2 ON WORD DRIVERS |
| ▼ | VSSXS | NEGATIVE VOLTAGE SUPPLY FOR SOURCE ON WORD DRIVERS |
| ▽ | VSSXW | NEGATIVE VOLTAGE SUPPLY FOR WELL ON WORD DRIVERS |
| ○ | VPPY | Y-SW & Z-SW SUPPLY |
| ① | VCC1 | LEVEL-SHIFTER SUPPLY |
| ⊗ | VCCSA | SENSE AMPLIFIER SUPPLY |
| ◍ | VPPW | PROGRAMMING CIRCUIT SUPPLY |
| ▽ | VSSE | NEGATIVE VOLTAGE SUPPLY FOR CONTROLLING Z-SW, SUBSTRATE AND SOURCE |

# FIG. 10

| STATE | X-DEC | | | | Y-DEC & Z-DEC | LEVEL-SHIFT | SENSE AMLIFIER | PROGRAMMING CIRCUIT | Z-SW & SOURCE & SUBSTRATE |
|---|---|---|---|---|---|---|---|---|---|
| | HIGH | | LOW | | HIGH | | | HIGH | LOW |
| | VPPX1 | VPPX2 | VSSXS | VSSXW | VPPY | VCC1 | VCCSA | VPPW | VSSE |
| PROGRAMMING | GND | VfixA (Vsft) | −9.5V (∗2) | −9.5V (∗2) | 9.5V (∗1) | VfixA (Vsft) | VfixA (Vsft) | 6.5V (∗1) | GND |
| PROGRAMMING SETUP | Vsft⇔GND | VfixA (Vsft) | GND⇔−9.5V (BOOSTING) | GND⇔−9.5V (BOOSTING) | Vcc⇔9.5V (BOOSTING) | VfixA (Vsft) | VfixA (Vsft) | Vcc⇔6.5V (BOOSTING) | GND |
| ERASURE | 9.5V (∗1) | 9.5V (∗1) | GND | GND | VfixA (Vsft) | VfixA (Vsft) | VfixA (Vsft) | Vcc | −9.5V (∗2) |
| ERASURE SETUP | Vcc | Vcc | GND | GND | VfixA (Vsft) | VfixA (Vsft) | VfixA (Vsft) | Vcc | −9.5V (∗2) |
| PROGRAMMING VERIFY | VfixA (Vsft) | VfixA (Vsft) | GND | GND | VfixA (Vsft) | VfixA (Vsft) | VfixA (Vsft) | Vcc | GND |
| ERASE VERIFY | 6.5V (∗1) | 6.5V (∗1) | GND | GND | VfixA (Vsft) | VfixA (Vsft) | VfixA (Vsft) | Vcc | GND |
| READ | VfixA (Vread) | VfixA (Vread) | GND | GND | Vcc | VfixA (Vread) | Vcc | Vcc | GND |
| | VfixA (Vread) | VfixA (Vread) | GND | GND | Vcc | VfixA (Vread) | Vcc | Vcc | GND |

∗1 : POSITIVE BOOSTING

∗2 : NEGATIVE BOOSTING

FIG. 11

| | VPPX1 | VPPX2 | VSSXS | VSSXW | VPPY | VCC1 | VCCSA | VPPW | VSSE |
|---|---|---|---|---|---|---|---|---|---|
| 9.5V (*1) | ● | ● | | | ● | | | | |
| 6.5V (*1) | ● | ● | | | | | | ● | |
| Vcc | ● | ● | | | ● | ● | ● | ● | |
| VfixA | ● | ● | | | ● | ● | ● | | |
| GND | ● | | ● | ● | | | | | ● |
| −9.5V (*2) | | | ● | ● | | | | | ● |

*1 : POSITIVE BOOSTING
*2 : NEGATIVE BOOSTING

FIG. 12

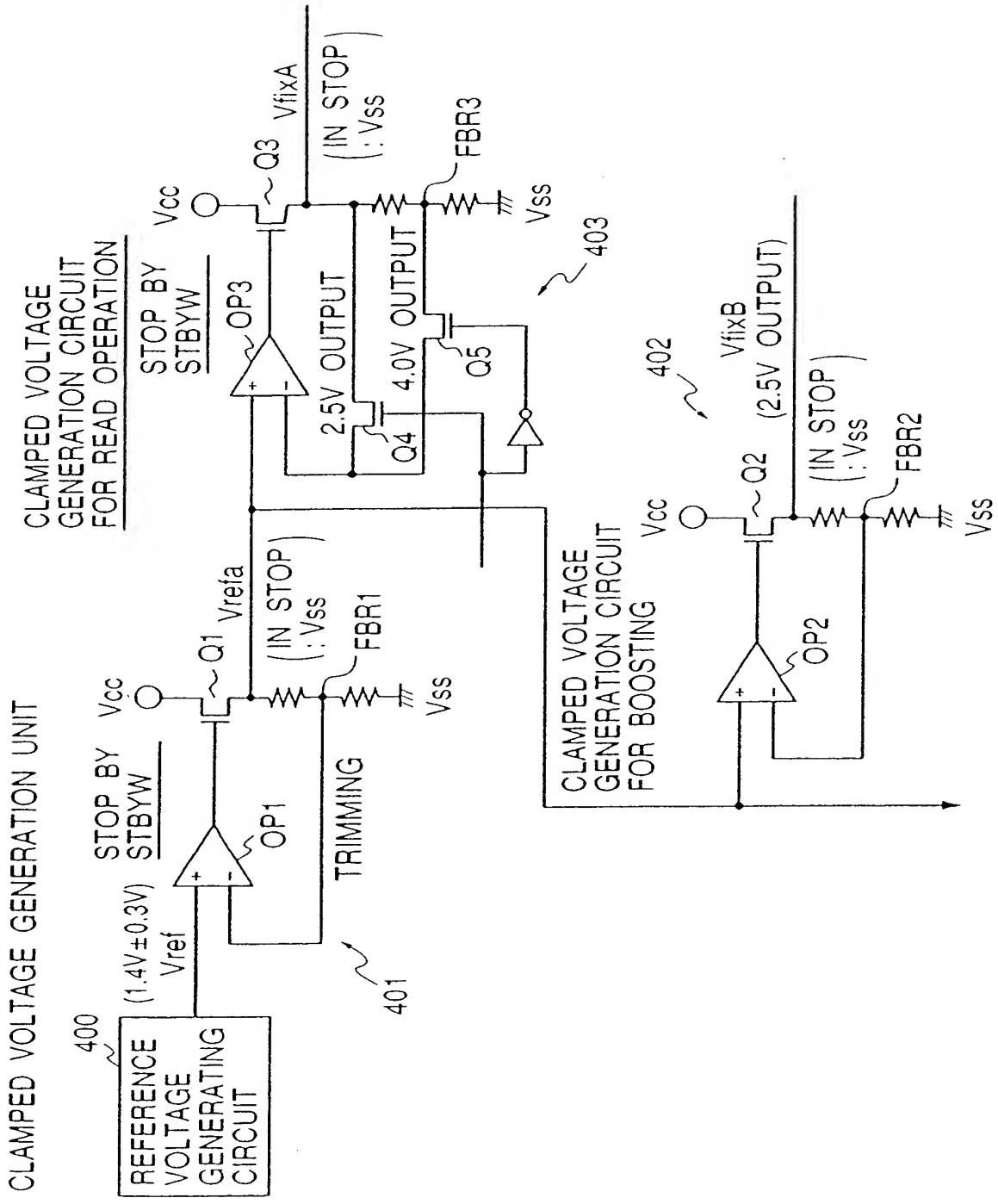

CLAMPED VOLTAGE GENERATION UNIT
400
REFERENCE VOLTAGE GENERATING CIRCUIT
(1.4V±0.3V)
Vref
STOP BY STBYW
Vcc
Q1
Vrefa
OP1
TRIMMING
401
FBR1
(IN STOP : Vss)
Vss
CLAMPED VOLTAGE GENERATION CIRCUIT FOR READ OPERATION
STOP BY STBYW
Vcc
Q3
VfixA
OP3
2.5V OUTPUT
Q4
4.0V OUTPUT
Q5
FBR3
(IN STOP : Vss)
Vss
403
CLAMPED VOLTAGE GENERATION CIRCUIT FOR BOOSTING
402
Vcc
Q2
VfixB
(2.5V OUTPUT)
OP2
FBR2
(IN STOP : Vss)
Vss

FIG. 13

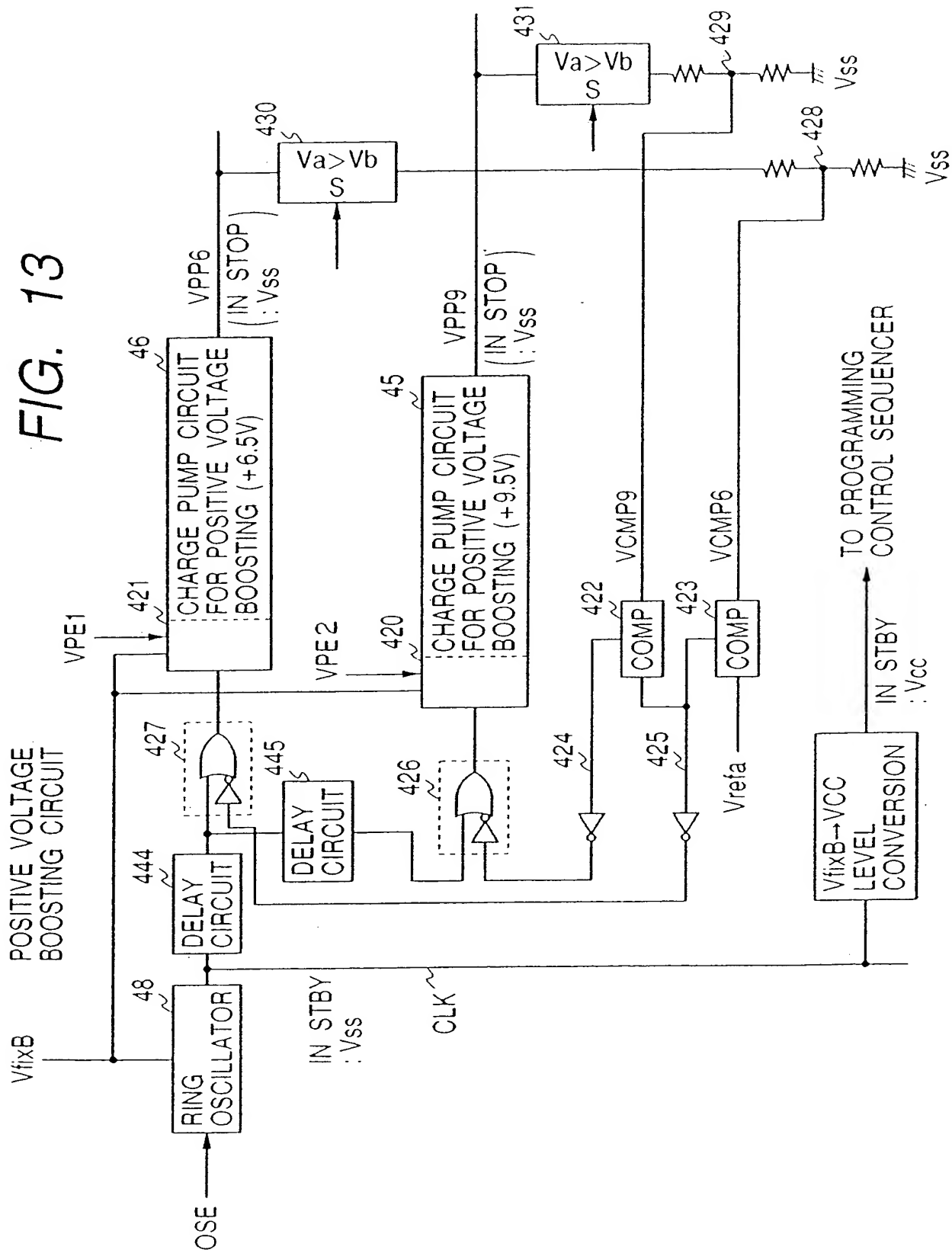
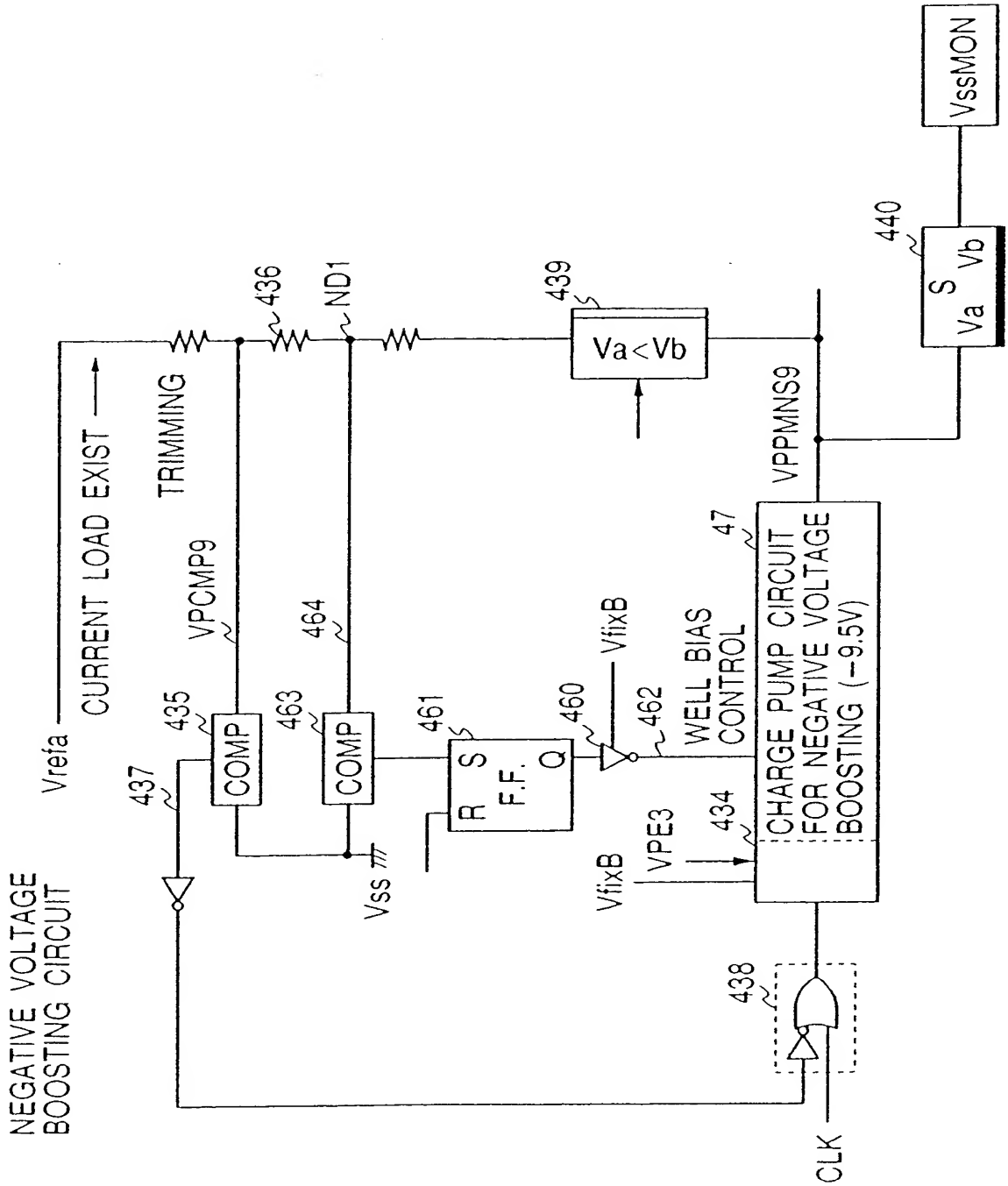
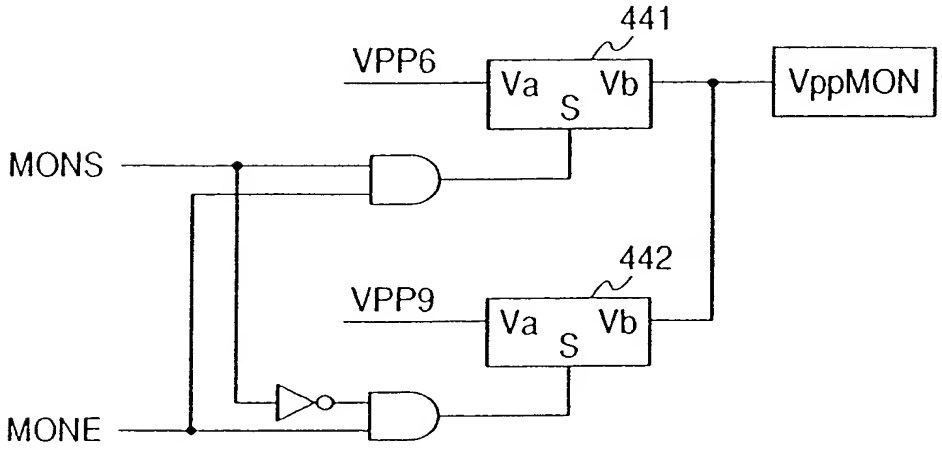

POSITIVE VOLTAGE BOOSTING CIRCUIT
VfixB
OSE
48
RING OSCILLATOR
444
DELAY CIRCUIT
427
445
DELAY CIRCUIT
426
424
425
Vreta
VPE1
421
CHARGE PUMP CIRCUIT FOR POSITIVE VOLTAGE BOOSTING (+6.5V)
46
VPP6
(IN STOP : Vss)
VPE2
420
CHARGE PUMP CIRCUIT FOR POSITIVE VOLTAGE BOOSTING (+9.5V)
45
VPP9
(IN STOP : Vss)
IN STBY : Vss
CLK
430
Va>Vb
S
431
Va>Vb
S
429
428
Vss
Vss
422
COMP
VCMP9
423
COMP
VCMP6
VfixB→VCC LEVEL CONVERSION
IN STBY : Vcc
TO PROGRAMMING CONTROL SEQUENCER

FIG. 14


NEGATIVE VOLTAGE BOOSTING CIRCUIT
Vrefa
CURRENT LOAD EXIST
TRIMMING
436
ND1
439
Va<Vb
440
S
Va
Vb
VssMON
VPPMNS9
VPCMP9
464
435
463
COMP
COMP
461
R S
F.F.
Q
460
VfixB
462
WELL BIAS CONTROL
47
CHARGE PUMP CIRCUIT FOR NEGATIVE VOLTAGE BOOSTING (−9.5V)
437
Vss
VfixB
VPE3
434
438
CLK

# FIG. 15

POSITIVE VOLTAGE MONITOR




# FIG. 16

REFERENCE VOLTAGE TRIMMING

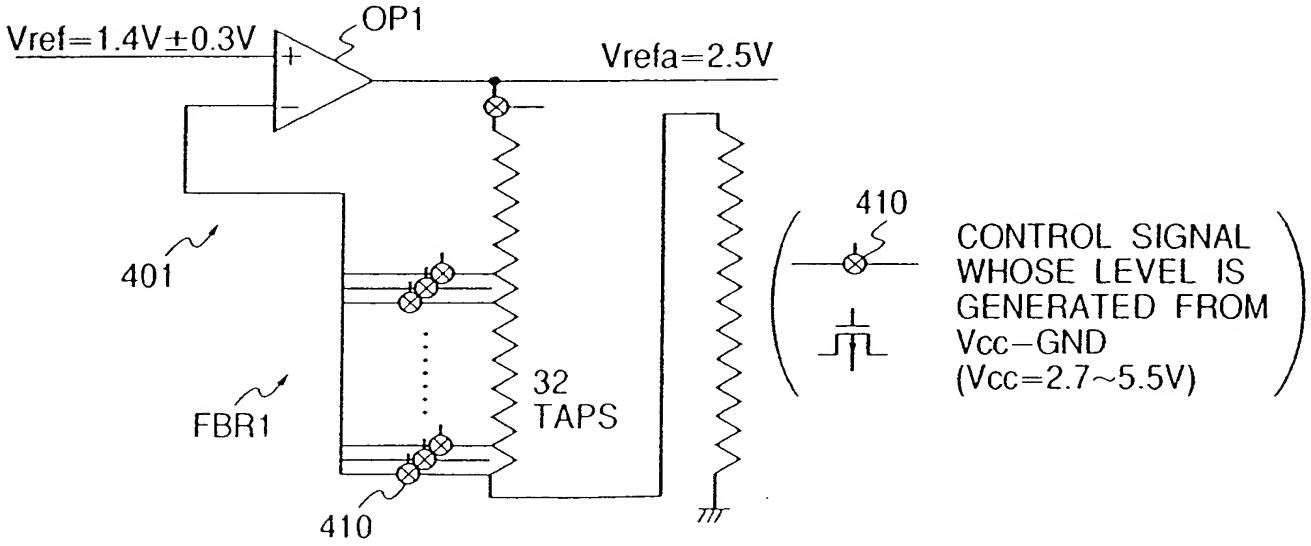


FIG. 17

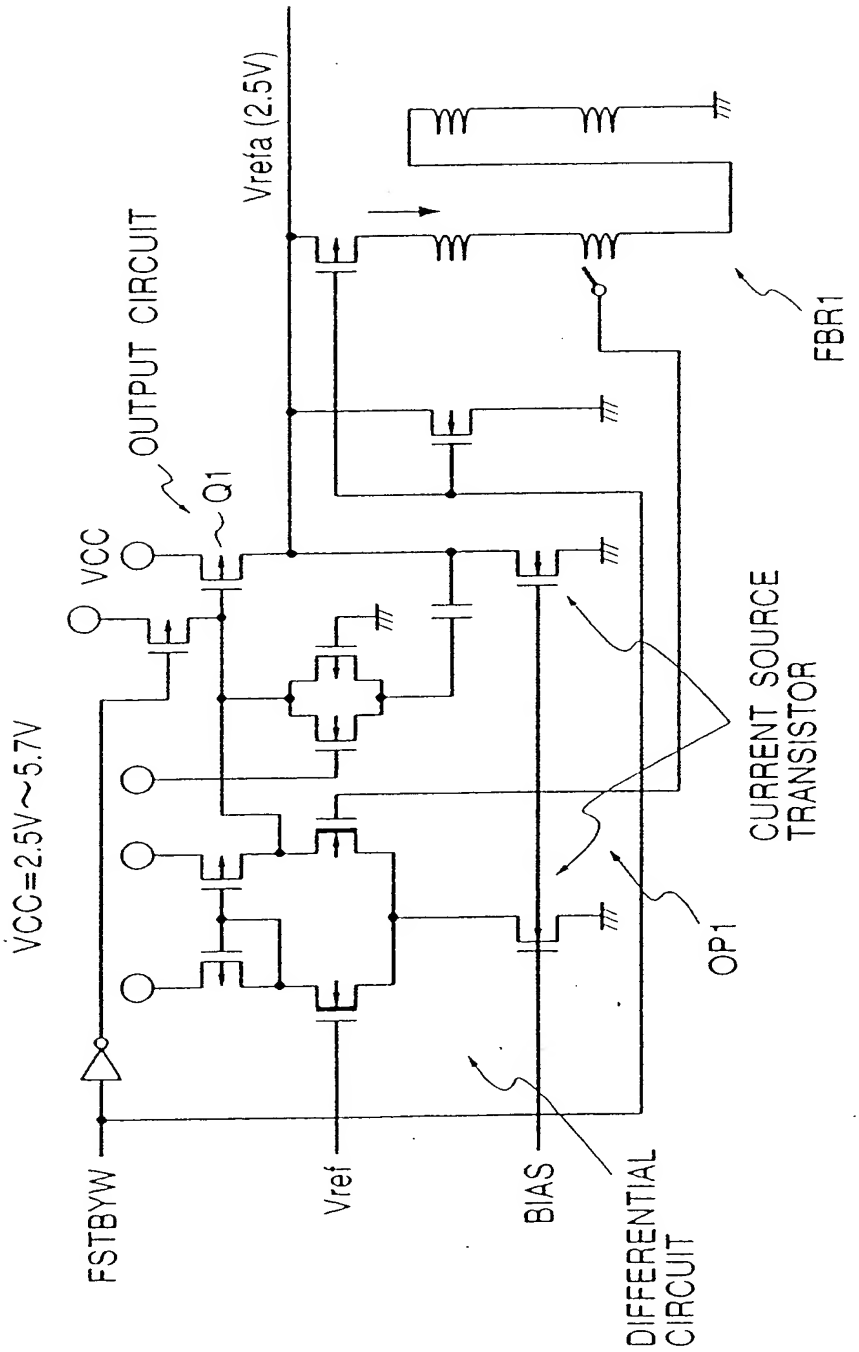
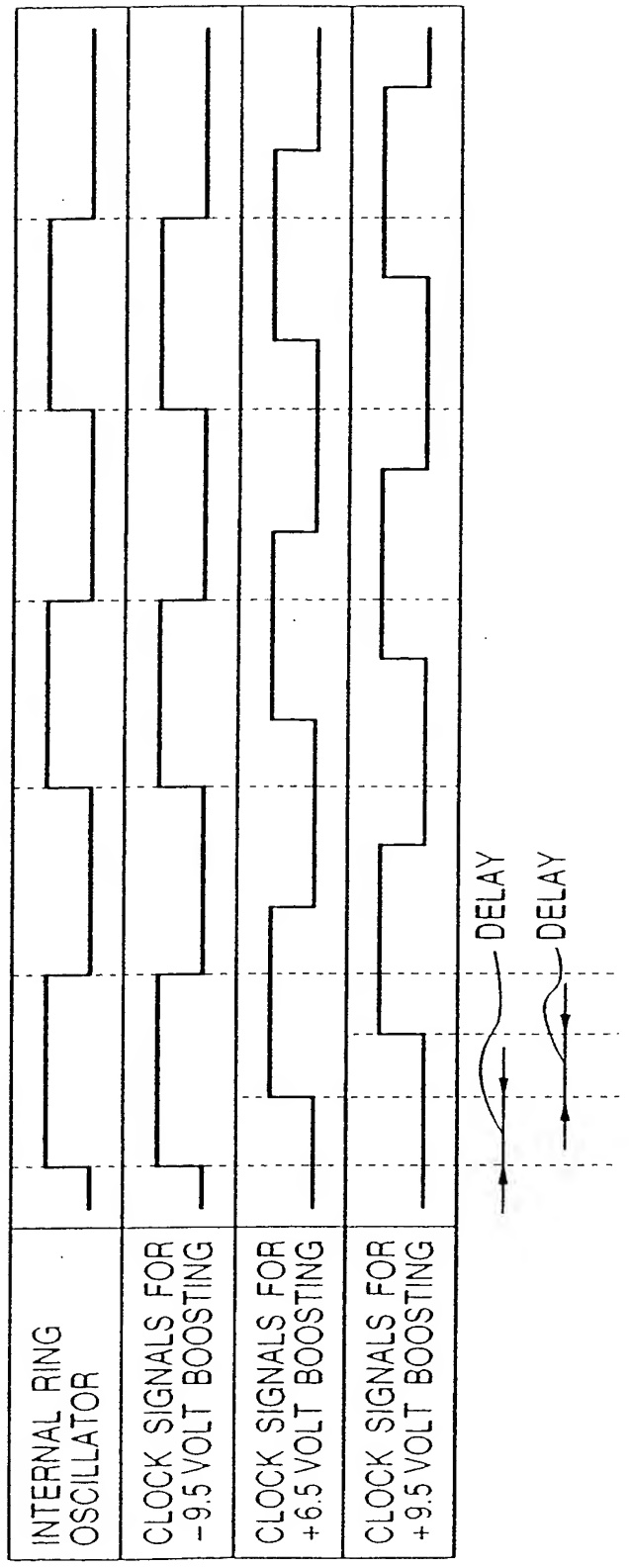

Vreta (2.5V)
OUTPUT CIRCUIT
Q1
VCC
VCC=2.5V~5.7V
FSTBYW
Vref
BIAS
DIFFERENTIAL CIRCUIT
CURRENT SOURCE TRANSISTOR
OP1
FBR1

FIG. 18


INTERNAL RING OSCILLATOR
CLOCK SIGNALS FOR −9.5 VOLT BOOSTING
CLOCK SIGNALS FOR +6.5 VOLT BOOSTING
CLOCK SIGNALS FOR +9.5 VOLT BOOSTING
DELAY
DELAY

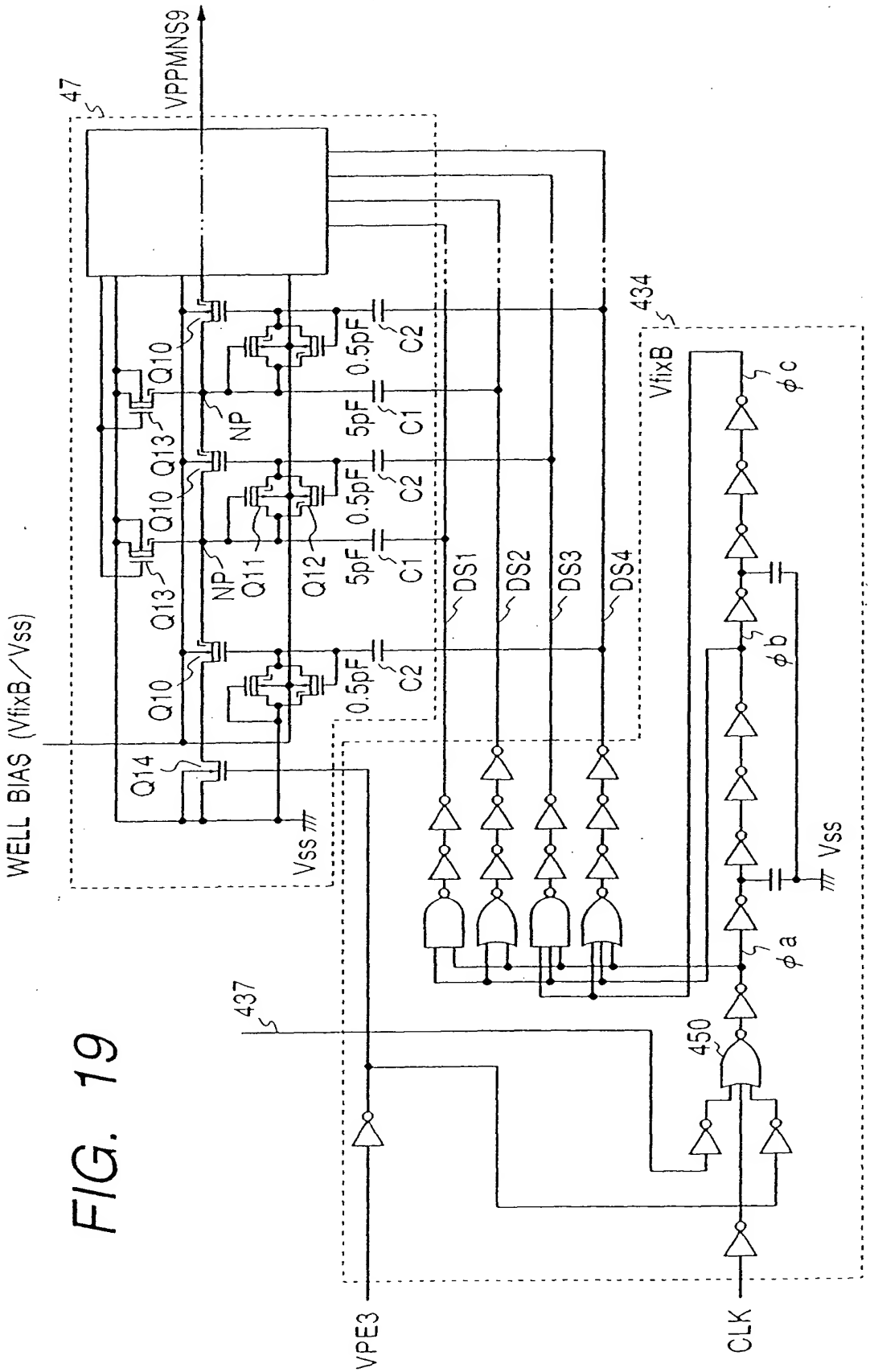

VPPMNS9
47
WELL BIAS (VfixB/Vss)
Q10
Q13
Q14
NP
Q11
Q12
0.5pF
5pF
C1
C2
DS1
DS2
DS3
DS4
Vss
434
VfixB
φc
φb
φa
437
450
VPE3
CLK

FIG. 19

FIG. 20

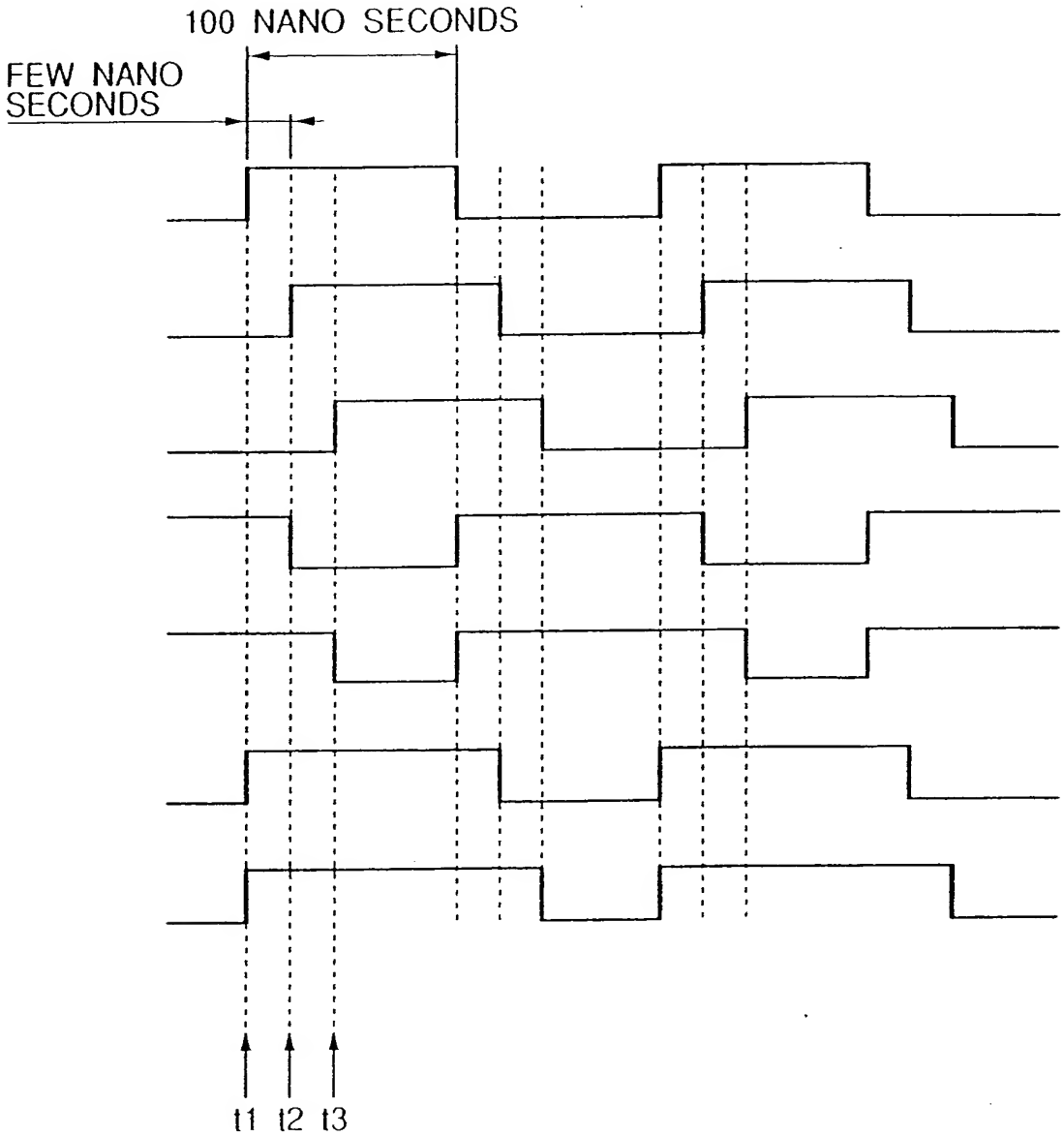


FIG. 21

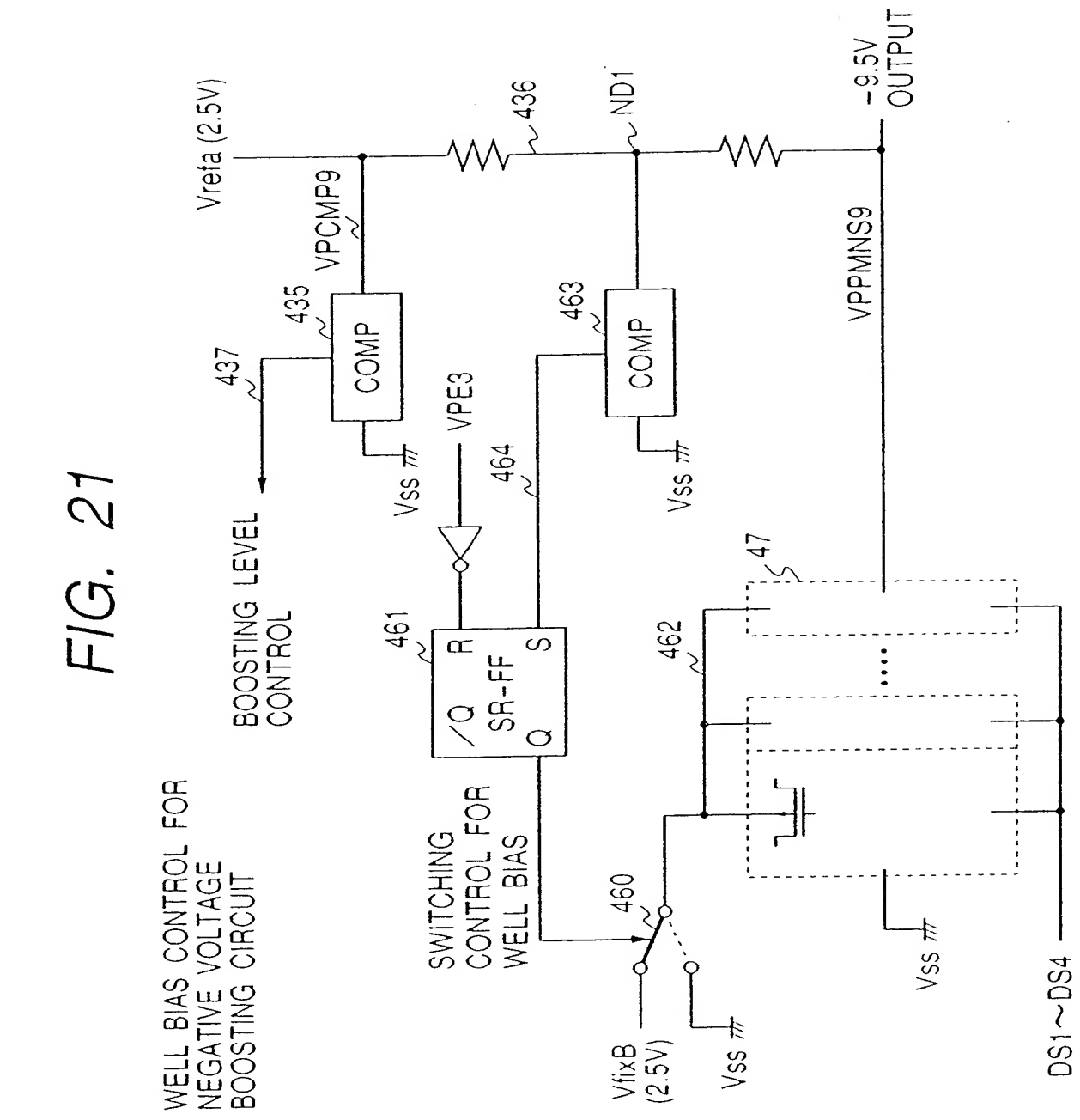

WELL BIAS CONTROL FOR
NEGATIVE VOLTAGE
BOOSTING CIRCUIT
BOOSTING LEVEL
CONTROL
SWITCHING
CONTROL FOR
WELL BIAS
Vreta (2.5V)
VPCMP9
436
ND1
-9.5V
OUTPUT
435
COMP
437
463
COMP
VPPMNS9
VPE3
464
Vss
461
R
/Q
SR-FF
S
Q
462
47
460
VfixB
(2.5V)
Vss
Vss
DS1~DS4

FIG. 22

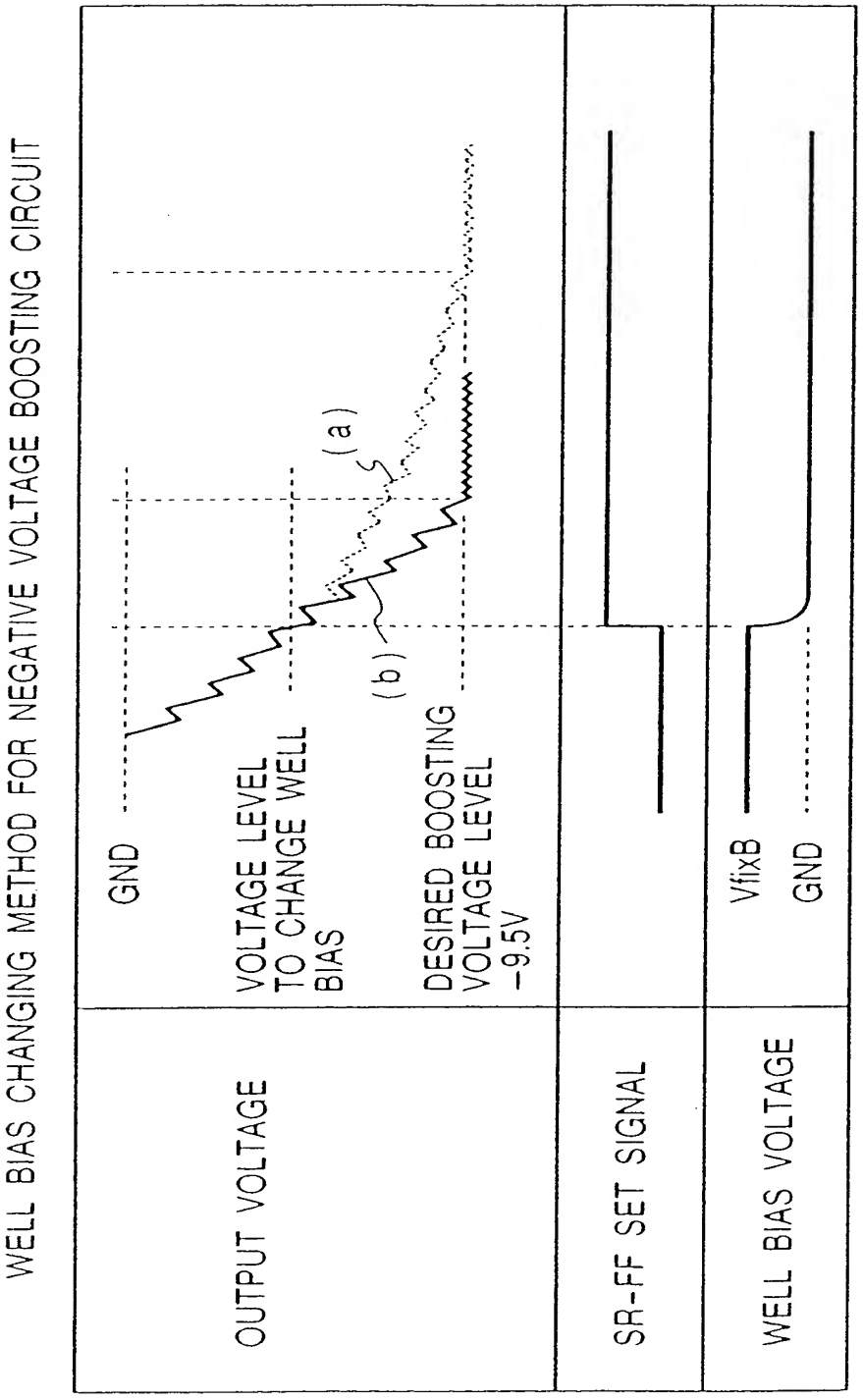

WELL BIAS CHANGING METHOD FOR NEGATIVE VOLTAGE BOOSTING CIRCUIT
OUTPUT VOLTAGE
SR-FF SET SIGNAL
WELL BIAS VOLTAGE
GND
VOLTAGE LEVEL TO CHANGE WELL BIAS
DESIRED BOOSTING VOLTAGE LEVEL −9.5V
(a)
(b)
VfixB
GND

FIG. 23

TRIMMING METHOD

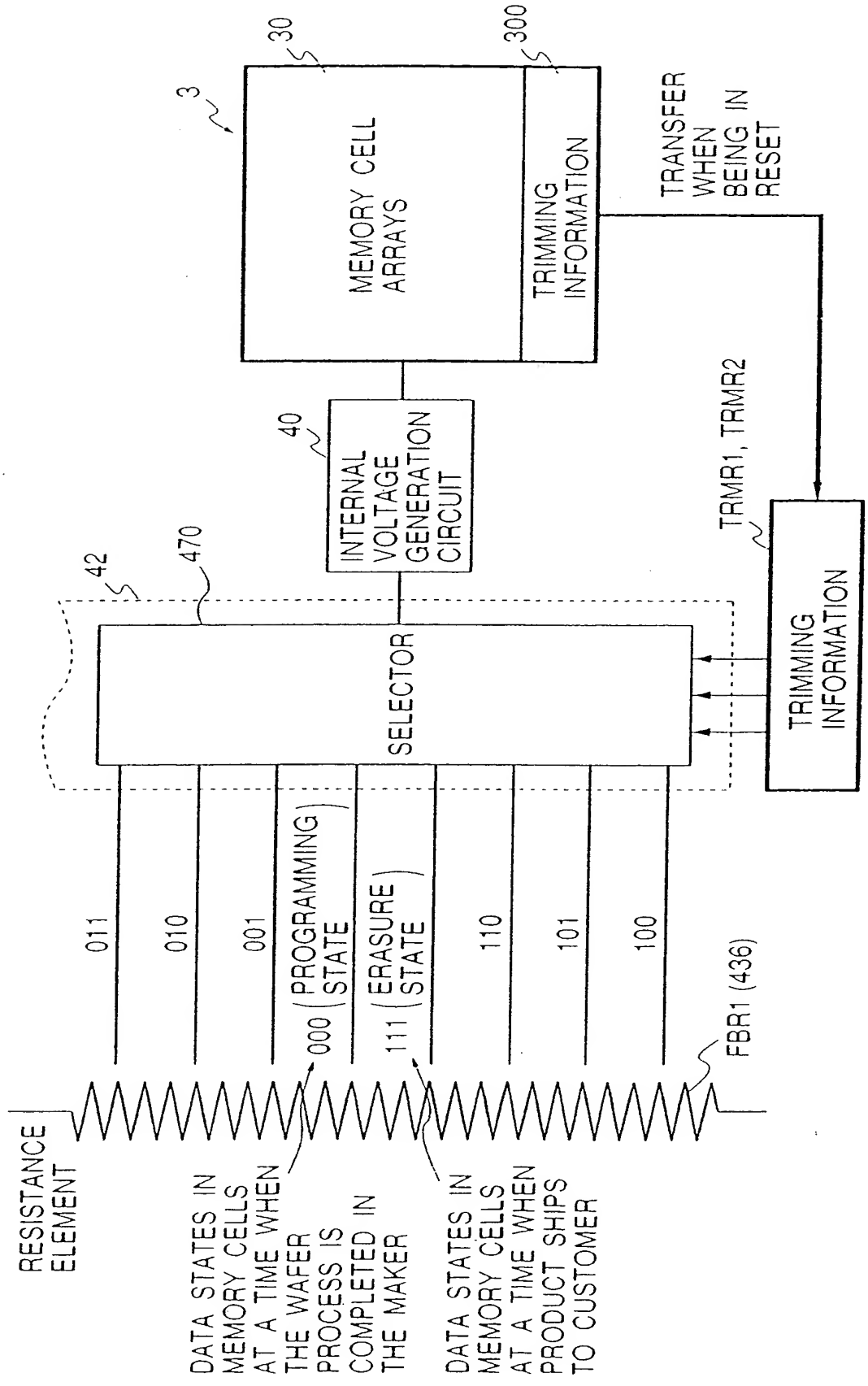


FIG. 24

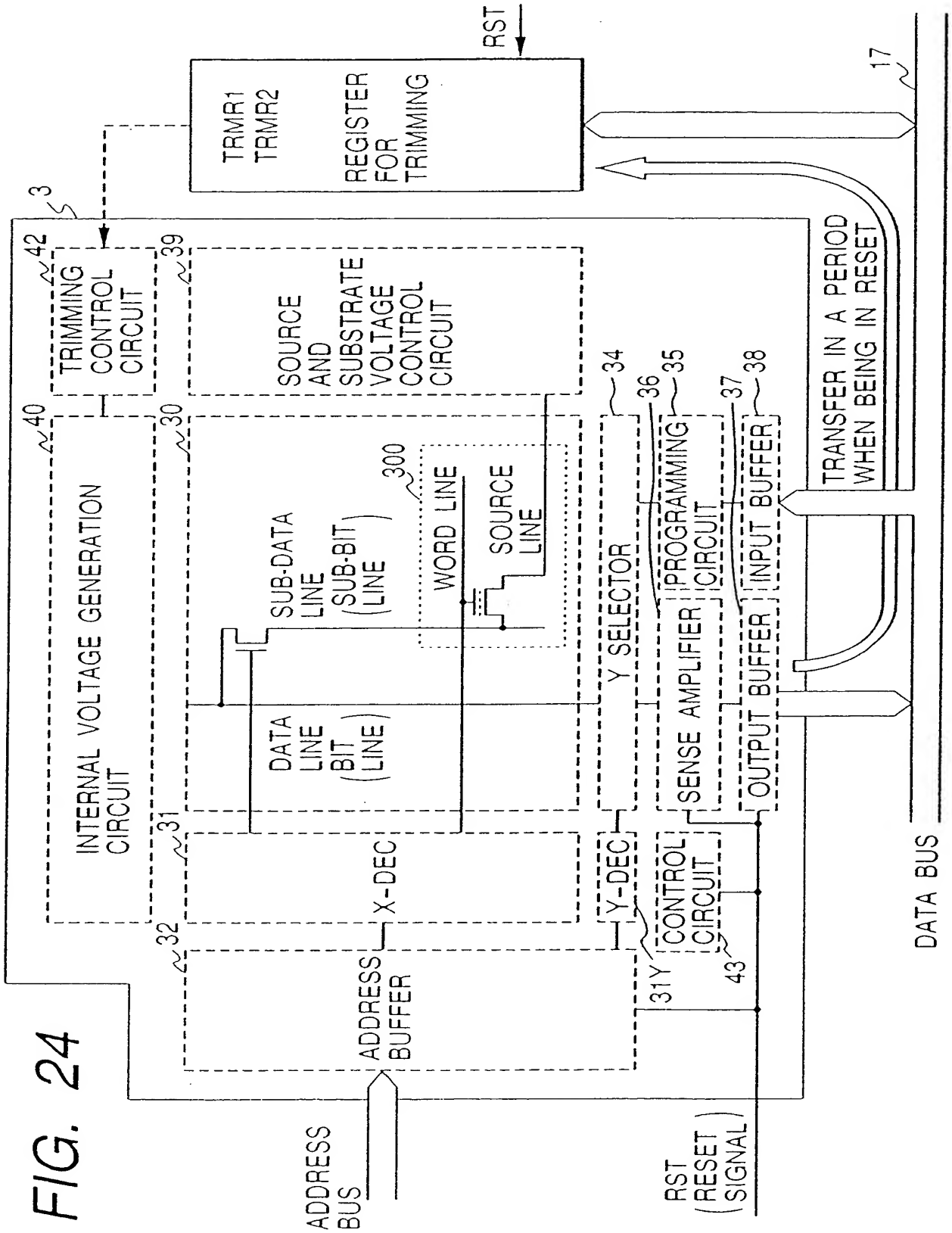

RST
TRMR1
TRMR2
REGISTER FOR TRIMMING
17
3
42
TRIMMING CONTROL CIRCUIT
39
SOURCE AND SUBSTRATE VOLTAGE CONTROL CIRCUIT
40
INTERNAL VOLTAGE GENERATION CIRCUIT
30
300
SUB-DATA LINE (SUB-BIT LINE)
WORD LINE
SOURCE LINE
DATA LINE (BIT LINE)
34
Y SELECTOR
36
35
PROGRAMMING CIRCUIT
37
38
INPUT BUFFER
SENSE AMPLIFIER
OUTPUT BUFFER
TRANSFER IN A PERIOD WHEN BEING IN RESET
31
X-DEC
Y-DEC
CONTROL CIRCUIT
32
ADDRESS BUFFER
31Y
43
DATA BUS
ADDRESS BUS
RST (RESET SIGNAL)

FIG. 25

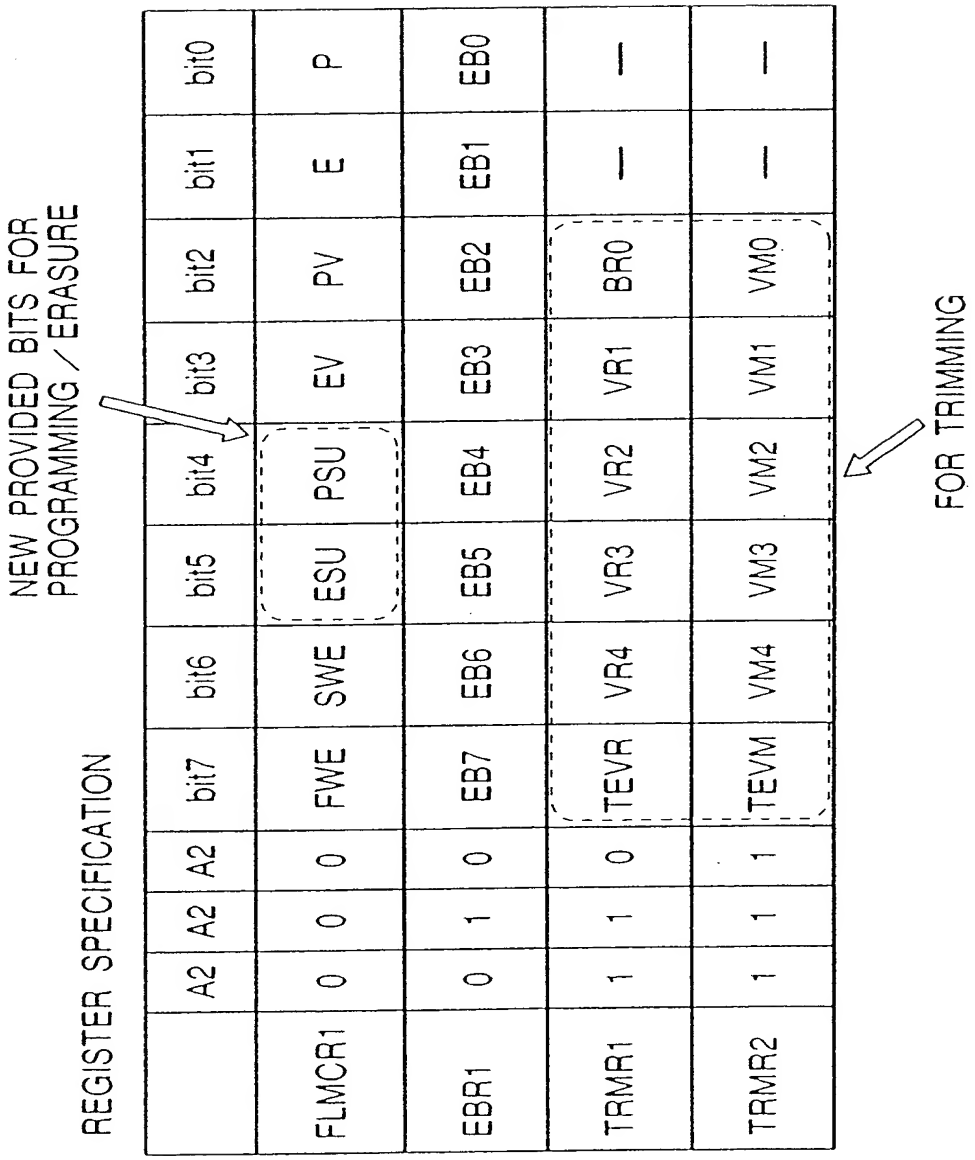

REGISTER SPECIFICATION
NEW PROVIDED BITS FOR PROGRAMMING / ERASURE
FOR TRIMMING
A2
A2
A2
bit7
bit6
bit5
bit4
bit3
bit2
bit1
bit0
FLMCR1
0
0
0
FWE
SWE
ESU
PSU
EV
PV
E
P
EBR1
0
1
0
EB7
EB6
EB5
EB4
EB3
EB2
EB1
EB0
TRMR1
1
1
0
TEVR
VR4
VR3
VR2
VR1
BR0
—
—
TRMR2
1
1
1
TEVM
VM4
VM3
VM2
VM1
VM0
—
—

FIG. 26

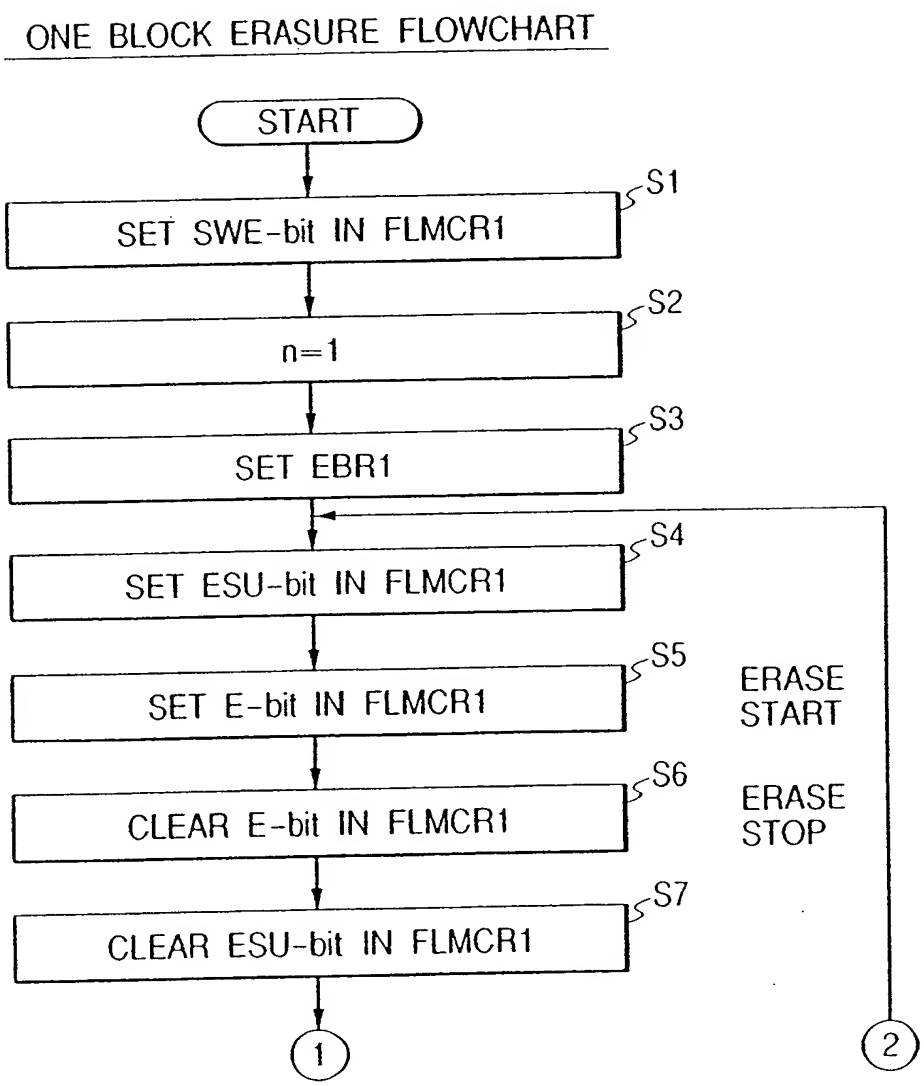

ONE BLOCK ERASURE FLOWCHART
START
S1
SET SWE-bit IN FLMCR1
S2
n=1
S3
SET EBR1
S4
SET ESU-bit IN FLMCR1
S5
SET E-bit IN FLMCR1
ERASE START
S6
CLEAR E-bit IN FLMCR1
ERASE STOP
S7
CLEAR ESU-bit IN FLMCR1
1
2

FIG. 27

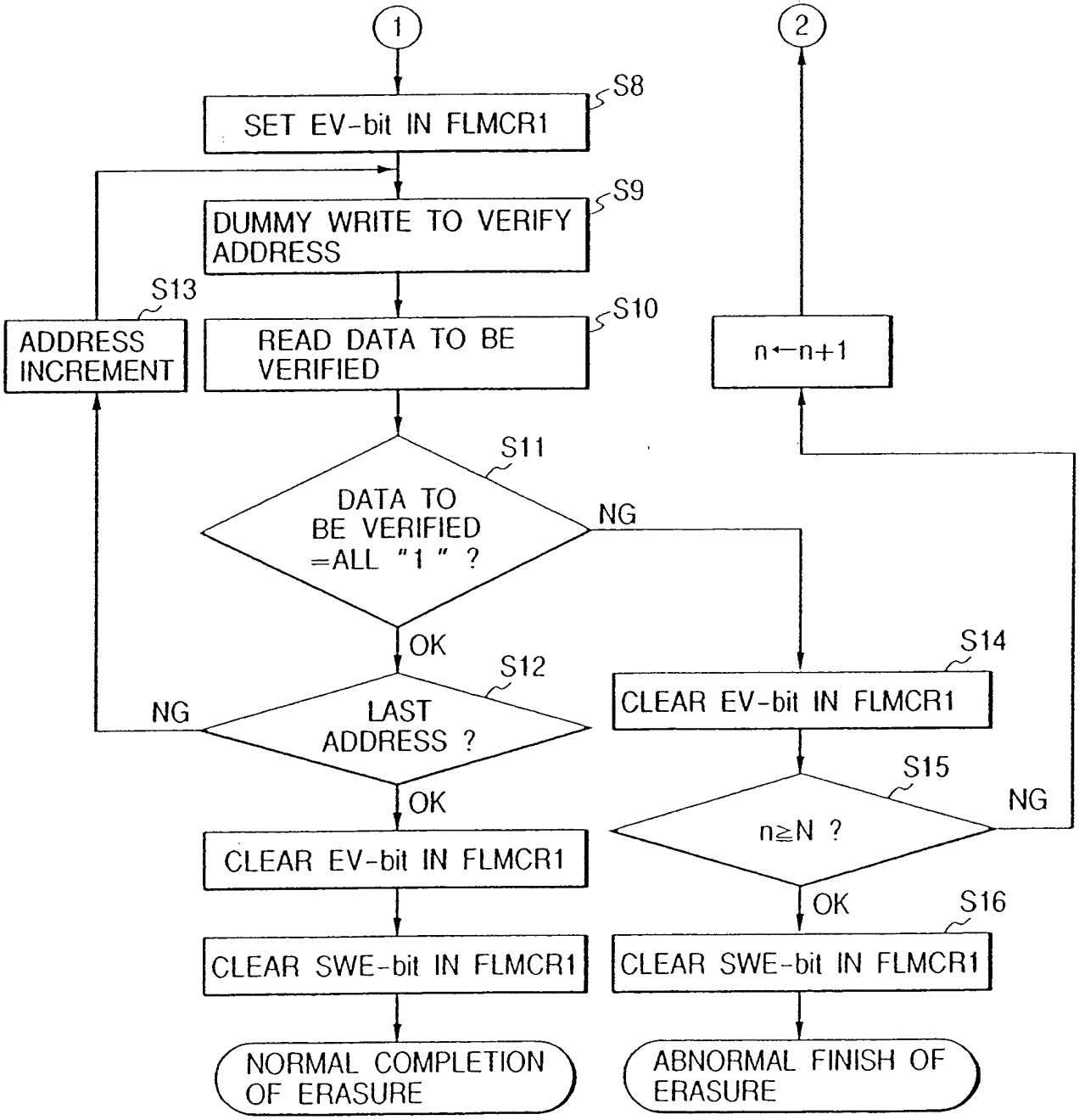

1
2
S8
SET EV-bit IN FLMCR1
S9
DUMMY WRITE TO VERIFY ADDRESS
S13
ADDRESS INCREMENT
S10
READ DATA TO BE VERIFIED
n←n+1
S11
DATA TO BE VERIFIED =ALL "1" ?
NG
OK
S12
NG
LAST ADDRESS ?
S14
CLEAR EV-bit IN FLMCR1
S15
NG
n≧N ?
OK
OK
S16
CLEAR EV-bit IN FLMCR1
CLEAR SWE-bit IN FLMCR1
CLEAR SWE-bit IN FLMCR1
NORMAL COMPLETION OF ERASURE
ABNORMAL FINISH OF ERASURE

FIG. 28

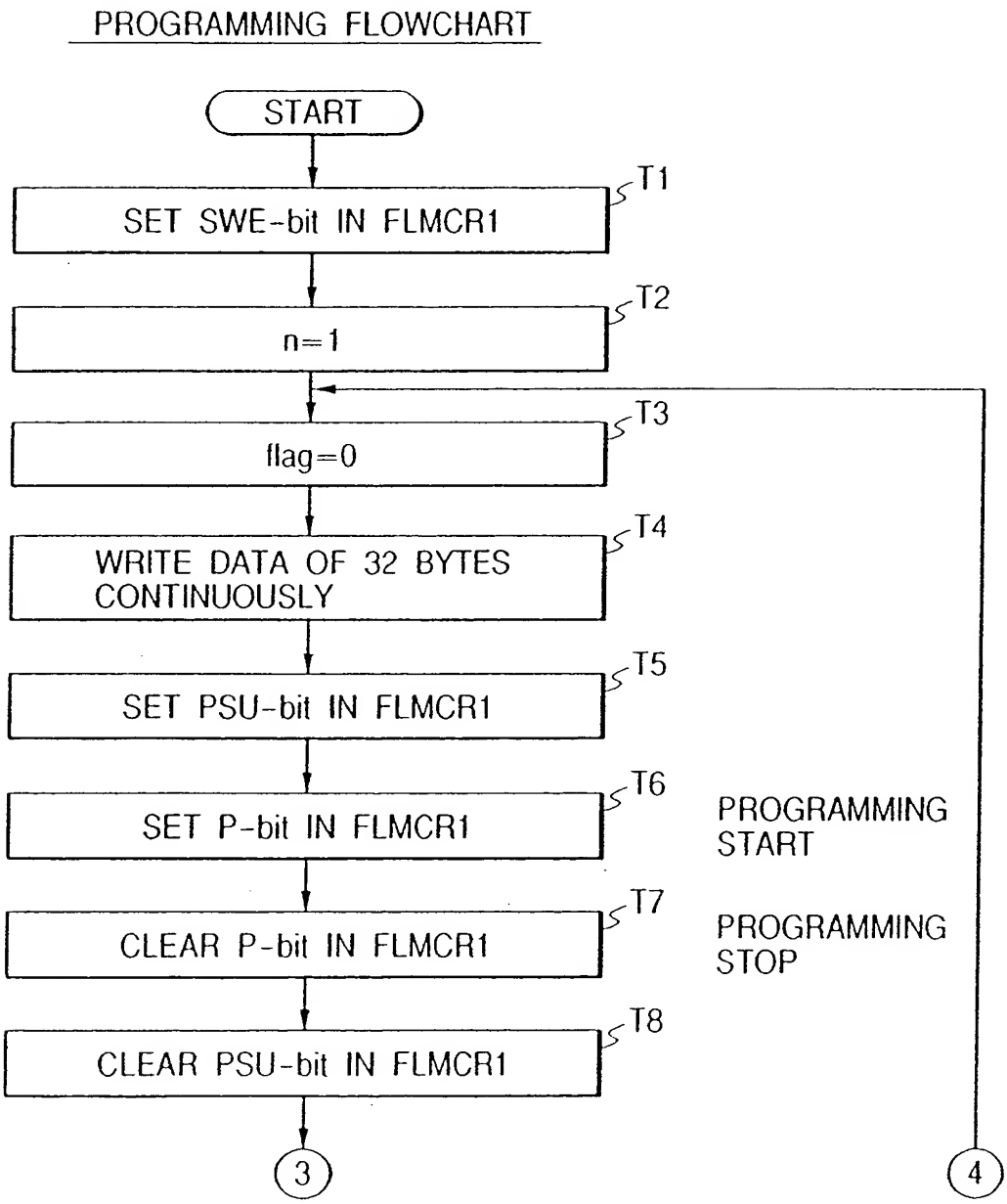
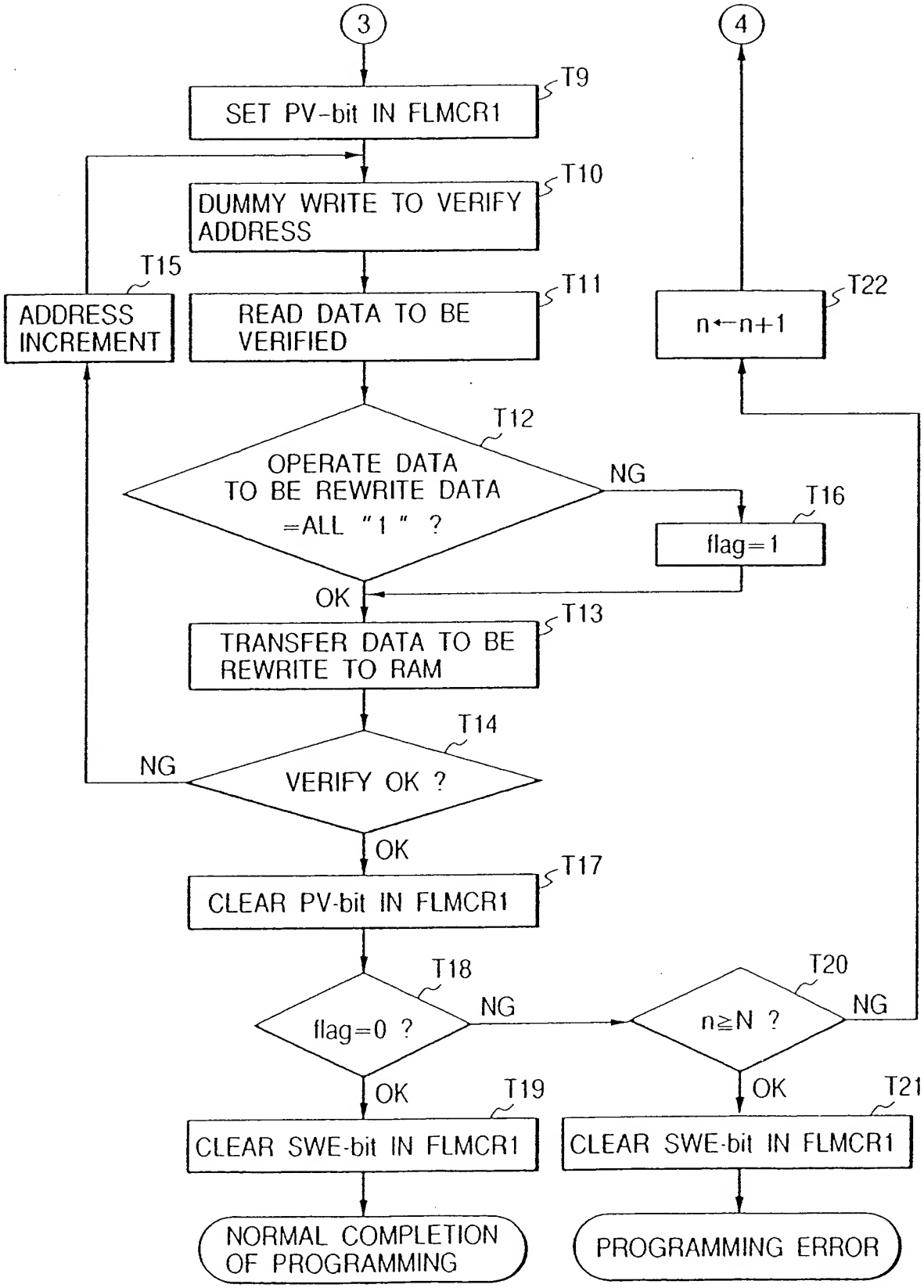

PROGRAMMING FLOWCHART
START
SET SWE-bit IN FLMCR1
T1
n=1
T2
flag=0
T3
WRITE DATA OF 32 BYTES CONTINUOUSLY
T4
SET PSU-bit IN FLMCR1
T5
SET P-bit IN FLMCR1
T6
PROGRAMMING START
CLEAR P-bit IN FLMCR1
T7
PROGRAMMING STOP
CLEAR PSU-bit IN FLMCR1
T8
3
4

FIG. 29

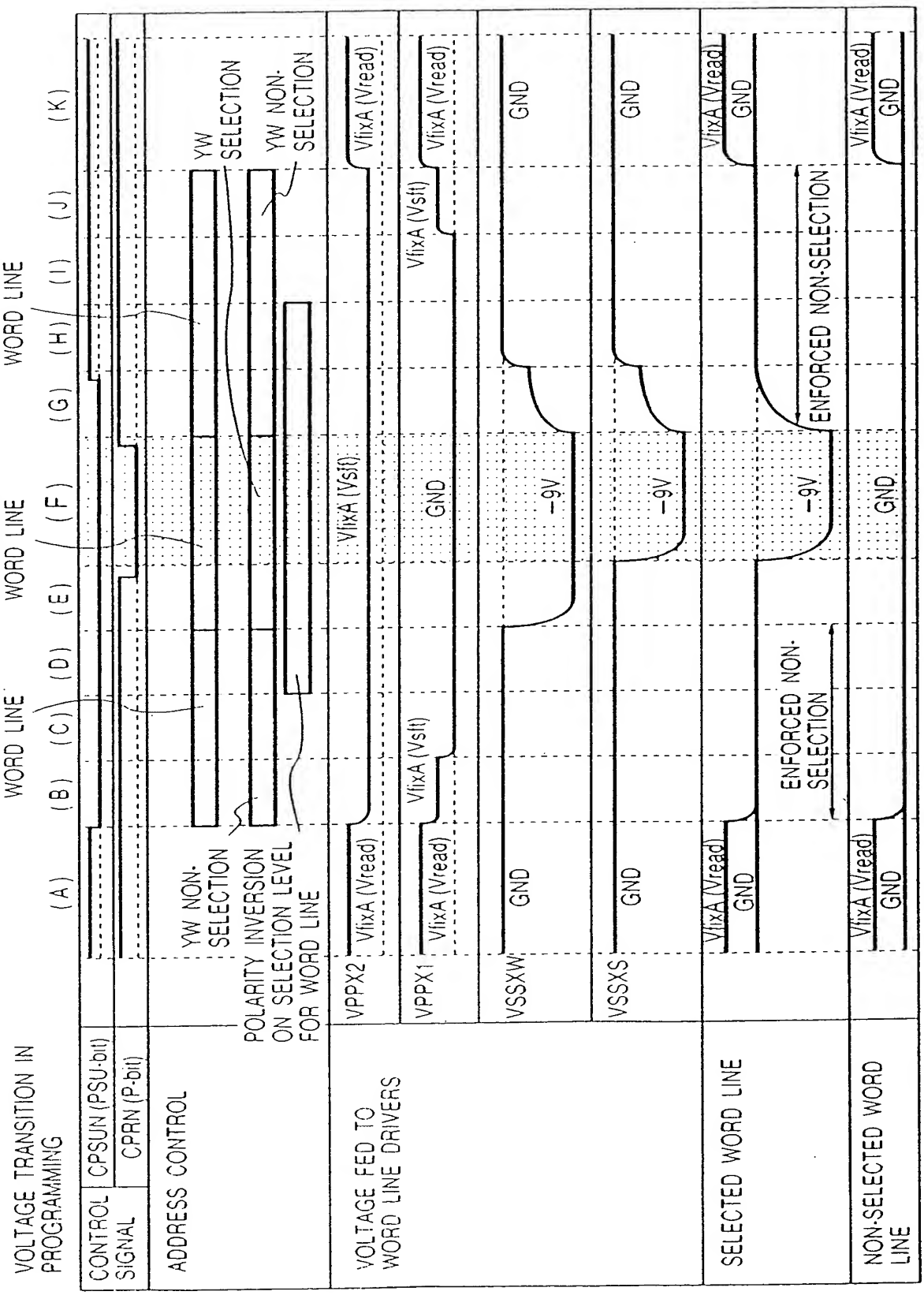

3
4
T9
SET PV-bit IN FLMCR1
T10
DUMMY WRITE TO VERIFY ADDRESS
T15
ADDRESS INCREMENT
T11
READ DATA TO BE VERIFIED
T22
n←n+1
T12
OPERATE DATA TO BE REWRITE DATA =ALL "1" ?
NG
T16
flag=1
OK
T13
TRANSFER DATA TO BE REWRITE TO RAM
T14
NG
VERIFY OK ?
OK
T17
CLEAR PV-bit IN FLMCR1
T18
flag=0 ?
NG
T20
n≧N ?
NG
OK
T19
OK
T21
CLEAR SWE-bit IN FLMCR1
CLEAR SWE-bit IN FLMCR1
NORMAL COMPLETION OF PROGRAMMING
PROGRAMMING ERROR

# FIG. 30

(*) ERASE STATE OF THE MEMORY CELL IS "1"
PROGRAMMING IS EXECUTED TO THE MEMORY CELL WHOSE STATE IS TO BE DATA "0"

| ORIGINAL PROGRAMMING DATA (D) | VERIFY DATA (V) | RE-PROGRAMMING DATA (X) | COMMENT |
|---|---|---|---|
| 0 | 0 | 1 | NO RE-PROGRAMMING IS EXECUTED TO THE MEMORY BIT THAT THE PROGRAMMING HAS BEEN COMPLETED |
| 0 | 1 | 0 | THE PROGRAMMING IS NOT COMPLETED, RE-PROGRAMMING IS EXECUTED |
| 1 | 0 | 1 | |
| 1 | 1 | 1 | ERASE STATE, NO PROGRAMMING IS EXECUTED |

FIG. 31


VOLTAGE TRANSITION IN PROGRAMMING
(A)
(B)
(C)
(D)
(E)
(F)
(G)
(H)
(I)
(J)
(K)
ENFORCED NON-SELECTION OF WORD LINE
SELECTION OF WORD LINE
ENFORCED NON-SELECTION OF WORD LINE
CONTROL SIGNAL
CPSUN (PSU-bit)
CPRN (P-bit)
ADDRESS CONTROL
YW NON-SELECTION
POLARITY INVERSION ON SELECTION LEVEL FOR WORD LINE
YW SELECTION
YW NON-SELECTION
VOLTAGE FED TO WORD LINE DRIVERS
VPPX2
VPPX1
VSSXW
VSSXS
VflxA (Vread)
VflxA (Vslt)
GND
-9V
SELECTED WORD LINE
NON-SELECTED WORD LINE
ENFORCED NON-SELECTION